	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	0	dockumaci near omer.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 17:45
2	BRS	L2	30	rengarajan near rajesh.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 17:45
3	BRS	L3	93	438/581.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 17:46

	Type	L #	Hits	Search Text	DBs	Time Stamp
4	BRS	L4	77664	(p-type) near15 (n-type)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 17:47
5	BRS	L5	1	(p-type) near15 (n-type near filed near effect near transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 17:47
6	BRS	L6	390	(p-type) near15 (n-type near field near effect near transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 17:47

	Type	L #	Hits	Search Text	DBs	Time Stamp
7	BRS	L7	8	((p-type) near15 (n-type near field near effect near transistor)) near35 ((sidewall$1 or side near wall$1 or spacer$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 17:50
8	BRS	L8	86	((p-type or pfet) near15 (n-type near field near effect near transistor or nfet)) near35 ((sidewall$1 or side near wall$1 or spacer$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 17:50
9	BRS	L9	20	((p-type or pfet) near15 (n-type near field near effect near transistor or nfet)) near35 ((sidewall$1 or side near wall$1 or spacer$1)) near25 ((remov$3 or pattern$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 18:07

	Type	L #	Hits	Search Text	DBs	Time Stamp
10	BRS	L10	2	((p-type or pfet) near15 (n-type near field near effect near transistor or nfet)) near35 ((sidewall$1 or side near wall$1 or spacer$1)) near25 ((remov$3 or pattern$3)) near35 ((silicide or salicide))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 18:11
11	BRS	L11	8	((p-type or pfet) near15 (n-type near field near effect near transistor or nfet)) near35 ((sidewall$1 or side near wall$1 or spacer$1)) near35 ((silicide or salicide))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 18:16
12	BRS	L12	8	((p-type or pfet) near15 (n-type near field-effect near transistor or nfet)) near35 ((sidewall$1 or side near wall$1 or spacer$1)) near35 ((silicide or salicide))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 18:16

	Type	L #	Hits	Search Text	DBs	Time Stamp
13	BRS	L13	19	((p-type or pfet) near15 (n-type near field-effect near transistor or nfet)) near35 ((silicide or salicide))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 18:20
14	BRS	L14	985	(transistor) near35 (remov$3 or pattern$3) near25 ((silicide or salicide))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 18:21
15	BRS	L15	87	(transistor) near35 ((remov$3 or pattern$3)) near10 ((spacer$1 or sidewall$1)) near25 ((silicide or salicide))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 18:27

	Type	L #	Hits	Search Text	DBs	Time Stamp
16	BRS	L16	19	(silicide) near25 (tensile) near25 (compress$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 18:28
17	BRS	L17	2	(silicide) near25 (tensile) near25 (compress$3) near25 (transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/08 18:28

	U	1	Document ID	Title	Current OR
1			US 6444531 B1	Disposable spacer technology for device tailoring	438/303
2			US 5647952 A	Chemical/mechanical polish (CMP) endpoint method	438/8
3			US 5643050 A	Chemical/mechanical polish (CMP) thickness monitor	451/10
4			US 5597442 A	Chemical/mechanical planarization (CMP) endpoint method using measurement of polishing pad temperature	438/8
5			US 5575706 A	Chemical/mechanical planarization (CMP) apparatus and polish method	438/693

	U	1	Document ID	Title	Current OR
6			US 20040140507 A	Formation of raised source/drain field effect transistor comprises growing boron-doped amorphous silicon on field effect transistor regions by selective epitaxy, forming abrupt source/drain junction and etching dual spacers in junction	
7	X		US 20030032295 A	Formation of raised source/drain field effect transistor involves growing boron doped amorphous silicon on n-type field effect transistor and p-type field effect transistor regions by selective epitaxy	
8	X		US 20020137341 A	Field effect transistor manufacturing method involves removing portions of silicon nitride and oxide layers to form spacers on sidewall of P-type and N-type field effect transistor gates, respectively	